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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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*Ex parte* STEPHEN R. VAN DOREN, GREGORY EDWARD TIERNEY, and SIMON C. STEELY JR.

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Appeal 2011-001054
Application 10/760,640[1]
Technology Center 2100

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*Before* LANCE LEONARD BARRY, JEAN R. HOMERE, AND JAY P. LUCAS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal from a final rejection of claims 1 to 9, 11 to 13, and 15 to 24 under authority of 35 U.S.C. § 134(a). Claims 10 and 14 are indicated as allowable if put into independent form. The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

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[1] Application filed January 20, 2004. The real party in interest is the Hewlett Packard Co.

We affirm-in-part.

Appellants' invention relates to a protocol for maintaining cache coherency in a computer. In the words of Appellants:

> Coherency protocols have been developed to ensure that whenever a processor reads a memory location, the processor receives the correct or true data. Additionally, coherency protocols help ensure that the system state remains deterministic by providing rules to enable only one processor to modify any part of the data at any one time. If proper coherency protocols are not implemented, however, inconsistent copies of data can be generated.
>
> There are two main types of cache coherency protocols, namely, a directory-based coherency protocol and a broadcast-based coherency protocol. A directory-based coherency protocol associates tags with each memory line. The tags can contain state information that indicates the ownership or usage of the memory line. The state information provides a means to track how a memory line is shared. Examples of the usage information can be whether the memory line is cached exclusively in a particular processor's cache, whether the memory line is shared by a number of processors, or whether the memory line is currently cached by any processor.
>
> A broadcast-based coherency protocol employs no tags. Instead, in a broadcast-based coherency protocol, each of the caches monitors (or snoops) requests to the system. The other caches respond by indicating whether a copy of the requested data is stored in the respective caches. Thus, correct ownership and usage of the data are

determined by the collective responses to the snoops.

SUMMARY

One embodiment of the present invention may comprise a system that includes a first node having an associated cache including data having an associated first cache state. The first cache state is capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data.

Another embodiment of the present invention may comprise a multiprocessor network that includes a plurality of processor nodes. Each processor node has at least one associated cache. The plurality of processor nodes employs a coherency protocol. The coherency protocol employs ordering points for serializing requests for data associated with the at least one associated cache of the plurality of processor nodes. The ordering point for the data is capable of being associated with the at least one associated cache of one of the processor nodes.

(Spec. 2, 3; ¶¶ [0004] to [0008]).

The following illustrates the claims on appeal:

Claim 1:

1. A system comprising:

a first node having an associated cache including data having an associated first cache state, the first cache state being capable of identifying the first node as being an ordering point for serializing requests from other nodes for the data.

Claim 7:

> 7. The system of claim 5, wherein the system implements a hybrid cache coherency protocol wherein each of the first and second processors employs a source broadcast-based protocol to issue a request for the data and employs an associated forward progress protocol to reissue a request for the data if the request fails in the source broadcast protocol.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

| | | |
|---|---|---|
| Arimilli | US 6,138,218 | Oct. 24, 2000 |
| Glasco | US 2005/0251626 A1 | Nov. 10, 2005 (filed on Apr. 24, 2003) |

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1 to 6, 11 to 13, 15 to 21 and 24 stand rejected under 35 U.S.C. § 102(e) for being anticipated by Glasco.

R2: Claims 7 to 9, 22 and 23 stand rejected under 35 U.S.C. § 103(a) for being obvious over Glasco in view of Arimilli.

We will review the rejections in the order argued and as grouped in the Briefs. We have only considered those arguments that Appellants actually raised in the Briefs. Arguments Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

## ISSUES

The pivotal issues before us are whether Appellants have shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e) and under 35 U.S.C. § 103(a). The issue under R1 specifically turns on whether Glasco teaches the order point for the serialization with the limitations in the various claims. The issue under rejection R2 turns on whether Arimilli teaches an associated forward progress protocol as claimed.

## FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellants have invented a protocol for maintaining coherency among the cache memories of multiple processors. (Spec. ¶ [0004]). Data in the caches is maintained in discreet states, indicating the reliability and other characteristics of the data. (¶ [0032]). Appellants disclose a hybrid coherency protocol using first broadcast snoop protocol (SSP), and then if that does not work, using the deterministic forward progress protocol (FPP). (¶ [0029]).

2. The Glasco reference teaches a cache coherency directory mechanism. (Fig. 7). The transfer ordering point is dependent on the state of the cache. (¶ [0090]).

3. Arimilli teaches retrying the snoop operations that failed to make forward progress on resolution. (Col. 1, l. 13; col. 5, l. 20).

PRINCIPLES OF LAW

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006) ("On appeal to the Board, an applicant can overcome a rejection [under § 103] by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness.") (quoting *In re Rouffet*, 149 F.3d 1350, 1355 (Fed. Cir. 1998)).

*See In re Jung*, 637 F.3d 1356, 1365, 1366 (Fed. Cir. 2011)("Jung argues that the Board gave improper deference to the examiner's rejection by requiring Jung to 'identif[y] a reversible error' by the examiner, which improperly shifted the burden of proving patentability onto Jung. *Decision* at 11. This is a hollow argument, because, as discussed above, the examiner established a prima facie case of anticipation and the burden was properly shifted to Jung to rebut it. . . . '[R]eversible error' means that the applicant must identify to the Board what the examiner did wrong . . . .").

The Court of Appeals for the Federal Circuit has cautioned against unreasonably broad claim construction:

> Although the PTO emphasizes that it was required to give all "claims their broadest reasonable construction" particularly with respect to [the] use of the open-ended term "comprising," *see Genentech, Inc. v. Chiron Corp.,* 112 F.3d 495, 501 (Fed. Cir. 1997) ("the open-ended term

> comprising ... means that the named elements are essential, but other elements may be added"), this court has instructed that any such construction be "*consistent with the specification,* ... and that claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Bond,* 910 F.2d 831, 833 (Fed. Cir. 1990). The PTO's construction here, though certainly broad, is unreasonably broad. The broadest construction rubric coupled with the term "comprising" does not give the PTO an unfettered license to interpret claims to embrace anything remotely related to the claimed invention. Rather, claims should always be read in light of the specification and teachings in the underlying patent. *See Schriber-Schroth Co. v. Cleveland Trust Co.,* 311 U.S. 211, 217 (1940).

*In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010).

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## ANALYSIS

*Arguments with respect to the rejection of claims 1 to 6, 11 to 13, 15 to 21 and 24 under 35 U.S.C. § 102(e) [R1]*

The Examiner has rejected the noted claims for being anticipated by Glasco. Appellants have raised a number of arguments.

With regard to claim 1, Appellants argue "Since Glasco teaches that the home memory controller is the serialization point for transactions to memory lines in the coherence directory regardless of the cache state for such memory lines, Glasco does not anticipate claim 1." (App. Br. 14, top). Further, "Stated differently, in claim 1, it is data in the associated cache of

the first node that identifies the first node as the ordering point, whereas in Glasco, it is the entries in a coherence directory of a memory controller for multiple processors that indicate the state of the line. Accordingly, Glasco does not anticipate claim 1." (App. Br. 15, bottom).

We have considered this argument, especially in light of the Examiner's reference to Glasco, ¶ [0087], ¶ [0089] and ¶ [0090]. These are just two of the many references in Glasco in which a node's ordering point is determined by the state of the cache. In ¶ [0087] the states are listed: modified, owned, shared and invalid. In ¶ [0089], reference is made to a dirty data owner information field, associated with address 781. In ¶ [0090] it is indicated that when the memory line is in a certain state (owned), the dirty data owner field is accessed to determine which cluster owns the dirty data. A further example is in ¶ [0095], where depending on being in the owned state, a remote cluster transmits the response back to the requesting cluster. Finally, in ¶ [0105], a "modified" memory state results in the transfer point being forwarded to the cluster owning the memory line.

In view of the breadth of the claim, we do not find error in the Examiner's rejection of anticipation over Glasco.

With regard to claims 2 and 4, the Appellants argue that Glasco describes the cited actions as involving a write-back to memory, contrary to the limitations of the claims. (App. Br. 16, middle). We agree with this argument. Considering the Examiner citation of ¶ [0116] and also of ¶ [0131], it is clear that the system memory in Glasco is being updated during the copy operations. As the limitations of the respective claims proscribe this memory update, we cannot sustain the rejection.

With regard to claim 3, the Appellants argue that Glasco does not teach "an ownership data response is provided that transfers an ordering point to another node." (App. Br. 17, bottom). We do not find error with the rejection for the reasons stated by the Examiner (Ans. 4, middle) supplemented as follows: In ¶ [0090], the dirty data ownership field indicates that another cluster owns the data. In ¶ [0095], the remote cluster transfers back the data. And in ¶ [0106], still another transfer is taught. All of these examples support the rejection.

With respect to claim 5, Appellants argue that the cache coherence controller 230 is used as a serialization point for processors of a multi-processor cluster. We have reviewed the Examiner's application of the Glasco art to the claim. (Ans. 5, top). We find all of the elements and limitations of the claim are resident in the art as claimed and do not find error in the Examiner's rejection.

*Arguments with respect to the rejection of claims 7 to 9, 22 and 23 under 35 U.S.C. § 103(a) [R3]*

The Examiner has rejected the noted claims for being obvious over Glasco in view of Arimilli.

Appellants argue that "[t]he approach taught in Arimilli does not provide for each processor to reissue a request for specific data by employing a forward progress protocol if the request fails in the source broadcast protocol, as recited in claim 7." (App. Br. 20, middle). We agree. The forward progress protocol is described carefully by the Appellants in the Specification, ¶ [0029]. While we will not read details of the Specification

into the claims, we will not accept interpretations of the terms of the claims that do violence to the meanings of those terms as used throughout the Specification. (*See Suitco Surface*, cited above.). It appears that the Examiner has found the terms "forward progress" in Arimilli and read those terms on the forward progress protocol. But the FPP of the Specification is related to the deterministic directory based protocol. (Spec 2). Arimilli is a multiple retry snooping protocol. We do not find this teaching sufficient to render obvious the use of a hybrid source broadcast protocol followed by a FPP deterministic protocol if the first protocol fails.

We find the Examiner erred in rejecting the noted claims under 35 U.S.C. § 103(a).

## CONCLUSIONS OF LAW

Based on the findings of facts and analysis above, we conclude that Appellants have shown that the Examiner erred in rejecting claims 2 and 4 under 35 U.S.C. § 102 and claims 7 to 9, 22 and 23 under 35 U.S.C. § 103(a). The remaining claims on appeal are properly rejected.

## DECISION

We reverse the Examiner's rejection R1 of claims 2 and 4 under 35 U.S.C. § 102(e).

We reverse the Examiners rejection R2 of claims 7 to 9, 22 and 23 under 35 U.S.C. § 103(a).

We affirm the Examiner's rejection R1 of the remaining claims under appeal.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

peb